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Low Power Methodologies for Improving and Targeting the Power-Intent Using Unified Power Format

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Abstract

As the Technology scales, loss of power in devices also goes on increasing, Dynamic loss of power due to switching action of the transistor states, so major challenge or key parameter is the Power, but power parameter should not affect the performance of the Device operation, so this Paper mainly focuses on the software implementation of the Design Targeting the power intent (UPF) and also demonstrates how the UPF models can be used to address the problems faced by the conventional adders in terms of area, power. The power intent is designed at relatively high level of hierarchy which describes which power rails must be routed to the specified block when required and the power is isolated from those unused blocks, as the signal crosses from one power domain to another power domain the power intent also describes the shift in voltage levels.

Keywords: Unified Power Intent, Conventional Carry Look ahead Adder, Hybrid Carry Look ahead Adder, Section Based Carry Look ahead Adder, Hybrid Section Based Carry Look ahead Adder

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1 Introduction

As we know that carry look ahead adder (CLA) is the fastest adder in adder family, due to the presence of the propagate and generate units, but this in turn also increases the power and Area of the devices [1]. The UPF plays an important central role in mitigating the dynamic and static power characteristics in the battle for low-power in the today's advanced VLSI process technology[2]. The higher process node is in general a definitely attractive as more and more functionality integration complexity is possible in a very smaller die area at a very lower cost[3]. However, in reality, this comes at the cost of exponentially increasing leakage power contributing to the total energy dissipation

In order to reduce the total Area a new adder is introduced called Section based carry look ahead adder (SCBCLA)[4,5,6]. And for power awareness, low power methodology like UPF is introduced in the Semi-Custom Mode of Implementation by using the Standard cells. And also in Different Hybrid designs. I.e. forming 32-bit adder using CCLA's and RCA, Similarly with SCBCLA in order to obtain the functionality of the designs and Their Figure of Merit (FOM) is tabulated individually.

2 Conventional Carry Lookahead Adder(CCLA)

As we know that CLA is the fastest adder, it consists of Generate (G) and Propagate (P) Units, Where Sum and Carry are obtained by Performing Different Operations Using Propagate and Generate Units[7,8,9]. The sum is obtained by Performing Logical XOR Operation using Propagate and Carry Bits. Similarly Carry is obtained by augend[2] and added inputs of the adder and are Expressed as in (1) and (2)

$$C_{i} = G_i + P_iC_i \quad (1)$$

$$Sum_i = P_i \oplus C_i \quad (2)$$

Here as Mentioned C and Sum Represents Fundamental Binary Addition Operation which is done by using Propagate and Generate Units where Gi=Ai Bi and Pi=Ai $\oplus$Bi , along with these it also results in generation of intermediate carries , i.e. look ahead carry outputs , C_1 , C_2 , C_3 and C_4 and are Given by the Relation

$$C_1 = G_0 + P_0C_0 \quad (3)$$

$$C_2 = G_1 + P_1G_0 + P_1P_0C_0 \quad (4)$$

$$C_3 = G_2 + P_2G_1 + P_2P_1G_0 + P_2P_1P_0C_0 \quad (5)$$

$$C_4 = G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1G_0 + P_3P_2P_1P_0C_0 \quad (6)$$

The Architectural Representation of general m-bit CCLA is represented in Fig. 1, it consist of three [3]basic blocks

a. Propagate and Generate unit
b. Carry look ahead unit
c. Summing unit

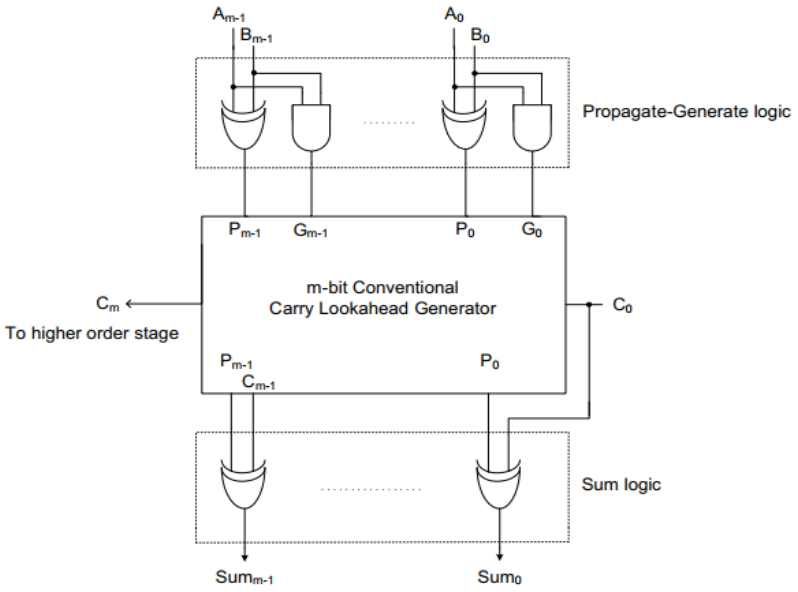


Fig. 1 Architecture of m-bit Conventional Carry Look ahead Adder

The CCLA structure is implemented using Verilog / VHDL . inorder to evaluate the results as per the requirements needed by the present CMOS technology , here by using this CCLA architecture different trails are carried out inorder to obtain the functionality of the CCLA with other stuctures and their behaviours are tabulated for performance.

3 Section Based Carry Look Ahead Adder

With the advent of CCLA and in order to obtain[10,11,12] the optimized less area than that the conventional CCLA. As the name suggest, it consists

of two operating section blocks , which are not at all connected to each other in order to get the optimized output.Hence, named a section based carry look ahead adder (SCBCLA) .

Here the production of sum is not at all dependent [13,14]on the carry from the look ahead sections. Hence it has only one look ahead output. The typical SCBCLA architecture is as shown in the Fig. 2. Here along with propagate and generate units it also has ripple carry adder (RCA) architecture. Which is designed only in order to obtain Sum outputs and carry is obtained from propagates and generates units.

If we observe Fig. 2 we can see that the carry output Cm is the derivative [15]that is obtained from generate and propagate unit and there is no other look ahead outputs apart from $C_{m\ from}$ Propagate and generate logic . Sum is obtained by using the logic of RCA. Thus it Results in less consumption of area since we are avoiding the look ahead carry bits which consumes large area which is the drawback to.

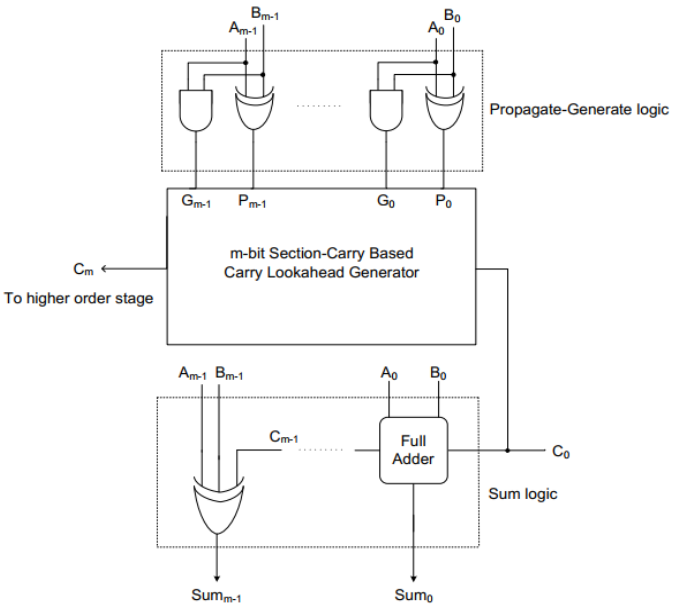


Fig . 2 Architecture of Section Based Carry Look ahead Adder

The architectures discuseed in section 2 and 3 with Conventional Carry Look ahead Adder and the Section Based Carry Look ahead Adder which are the fundamental adders which we are concerned about and by using these

adders we are building some complex designs and evaluating the behaviour of these adders .

4 Low Power Methodolgy

This is one of the most important concept on which the paper focuses mainly [15, 16] on low power improvements, nothing but Reduction of power by targeting UPF. UPF is basically an IEEE 1801 standard of defining the power intent which is used to introduce the low Power cells without changing the design and is abbreviated as Unified Power Format.

4.1 Power Dissipation in CMOS

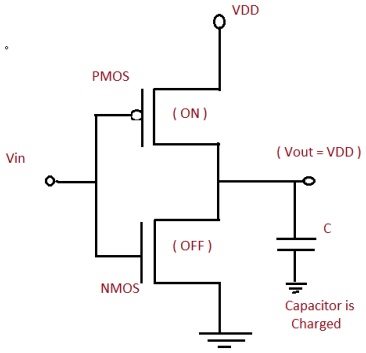
In digital design, The major problems are facing for all the devices in modern day technologies [17] mainly

1.Static power losses is the power loss in any CMOS circuit which happens even when the input or the output states of the device is constant or in valid logic level resulting in the leaking current and is very low but still resulting in power loss.

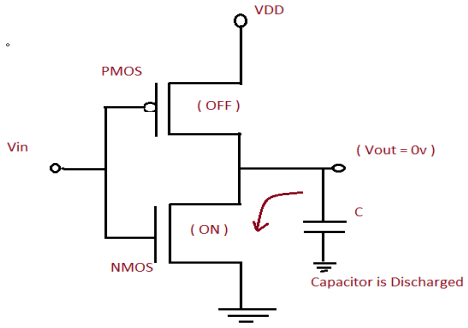
2. Dynamic loss is the power loss basically due to the repeated charging and discharing action of the load capacitence that takes place in any CMOS circuit and is expressed in (7).

$$P_{dynamic} = C_l \, VDD^2 \, \Omega \, F \qquad (7)$$

Where $P_{dynamic}$ = dynamic power loss
VDD^2 = supply Voltage
Ω = activity factor
F = clock frequency C_l = Load capacitance



(a)



(b)

Fig .3 a. shows Charging in CMOS Circuit b. shows Discharging in CMOS Circuit

The Diagrammatic Representation of Fig 3a and 3b, Represents how the charging and Discharging of the load capacitor in a CMOS circuit takes place. From equation (7) it is clear that the Power is directly proportional to the capacitance, supply, frequency, if we can decrease any one of these parameters then power decrease, which in turn decreases the performance of the system. The objective in the proposed paper is to reduce power [18] without affecting the Performance of the system is to use the Unified power format.

4.2 Unified Power Format

UPF is an IEEE standard Developed by Accellera in order to define the power intent. Where we can specify certain low power cells that are Isolation

cells, Retention cells, Level shifters etc., there are different methodology methods that can be used to reduce power

1. Power gating : it is nothing but switching off the power when it is not required
2. Clock Gating : switching off the clock circuitry when it is not required
3. Multi VDD: Different Voltage rails are introduced when multiple blocks are running in SOC's.

Apart from different methodologies we can use power switches in order to switch off or to gate the blocks and isolation cells in order to provide isolation between on and off domains, retentions cells are like memory cells which is used to store the values during gating, and this values might require when that block gets on. Level shifter plays a major role in varying the voltage as per required. This design doesn't Contains any clock circuitry and hence the concept of Clock gating is not used here. But Power gating [19]and formation of domain is the key parameter in the proposed design.

5 Design for Implementation

5.1Design Using CCLA Micro Architecture

As discussed discuseed in section I and II i.e., CCLA, SCBCLA, etc., by using conventional architecture [7,8,9]few designs are selected in order to evaluate the behavior of these adders. Fig.4 (a) represents the Hybrid CCLA_1, which means CCLA which is messed with other adders. Here 32 bit adder is Designed by combining seven 4 – bit CCLA's and 1 ripple carry adder of 4 bit, resulting 32 bit adder.

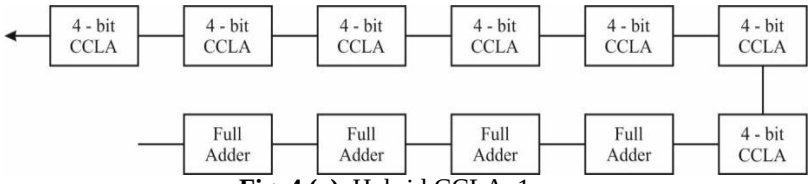


Fig. 4 (a) Hybrid CCLA_1

Fig.4 (a) represents the Hybrid CCLA_1, which means CCLA which is messed with other adders. Here 32 bit adder is Designed by combining seven 4 – bit CCLA's and 1 ripple carry adder of 4 bit, resulting 32 bit adder.

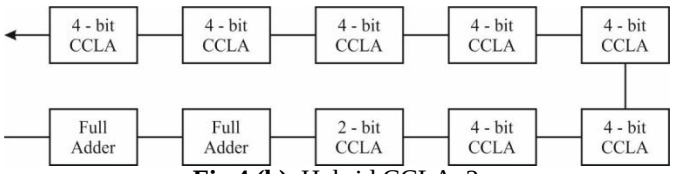


Fig.4 (b) Hybrid CCLA_2

Fig.4 (b) represents the Hybrid CCLA_2, which means CCLA which is messed with other adders. Here 32 bit adder is Designed by combining seven 4 – bit CCLA's and 1 ripple carry adder of 2 bit, resulting 32 bit adder.

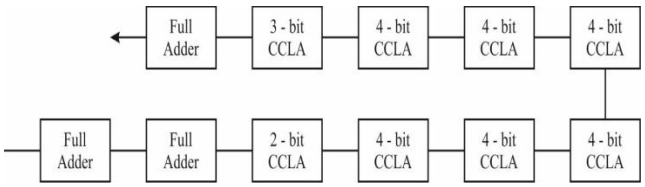


Fig.4 (c) Hybrid CCLA_3

Fig.4 (c) represents the Hybrid CCLA_3, which means CCLA which is messed with other adders. Here 32 bit adder is Designed by combining six 4 – bit CCLA's and two with 3-bit,2-bit CCLA and 1 ripple carry adder of 2 bit, resulting 32 bit adder.

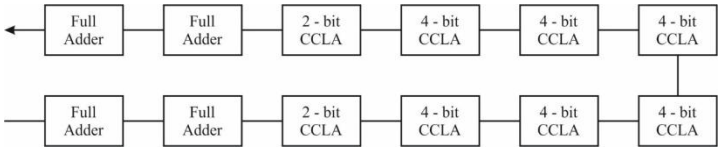


Fig . 4(d) Hybrid CCLA_4

Fig.4 (d) represents the Hybrid CCLA_4, which means CCLA which is messed with other adders. Here 32 bit adder is Designed by combining six 4 – bit CCLA's and with two,2-bit CCLA and 1 ripple carry adder of 4 bit, resulting 32 bit adder.

5.2 Design Using SCBCLA Micro Architecture

The 32-bit adder design is implemented [10,11] using SCBCLA architecture. Where the CCLA adder block in the previous section design is replaced by SCBCLA micro-architecture for performance evaluation. Fig.5 (a) represents the Hybrid SCBCLA_1, which means SCBCLA which is messed with other adders. Here 32 bit adder is Designed by combining seven 4 – bit CCLA's and 1 ripple carry adder of 4 bit, resulting 32 bit adder.

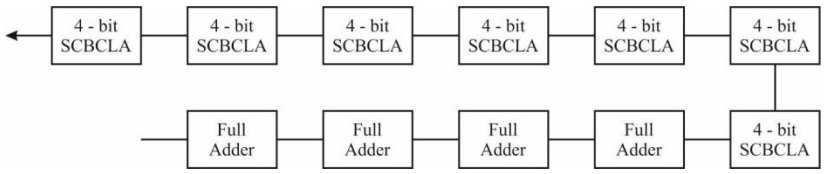


Fig. 5(a) Hybrid SCBCLA_1

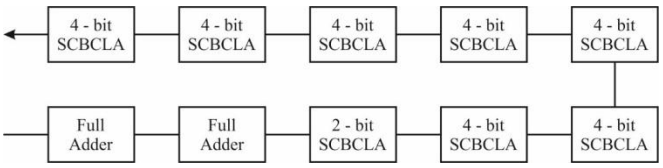


Fig.5(b) Hybrid SCBCLA_2

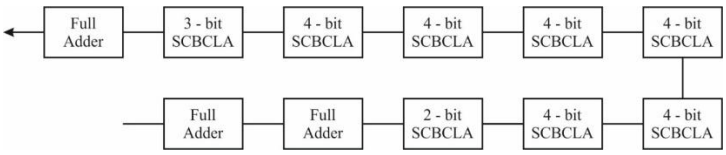


Fig.5(c) Hybrid SCBCLA_3

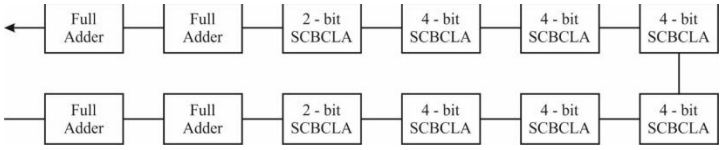


Fig. 5(d) Hybrid SCBCLA_4

Above Fig. 5(a),5(b),5(c) and 5(d) Represents the Adder design with SCBCLA as its architecture with possible combination to implement 32-bit adders , by using these architectures shown in fig.5 .The above design is implemented and its performance is computed and compared with the design obtained from CCLA architecture [11]in order to obtain better figure of merits.

6 Design Implementation using UPF

The very important objective is to implement UPF[15,16,17] for the particular designs as discussed in the previous sections using CCLA, SCBCLA architectures. The procedure to implement UPF is as follows:-

- Creation of Separate Power domains: This plays a major role, here we form a separate power domains such that separate supplies are taken to each domain as per Required, which in turn saves power. for e.g. if we consider 2 domains , domain 1 and domain 2 , suppose domain 1 needs 1.5V to operate and domain 2 needs 1V to operate so we can provide required voltages for a particular domain instead of wasting the power .

- Power Gating and Power switches :

This is the second important step which is nothing but insertion of Power switches in order to switch off or block whenever its functionality is not required. And this process is called power gating.

- Level Shifters :

These are very low power cells which is used within a particular block in order to vary the voltage value as per Requirement in the design i.e. voltage scaling.

- Isolation and Retention :

Isolation cells are the cells which are used for providing isolation for those blocks. for e.g. if block 1 is off and block 2 is on , there might be some chances that signals might pass from OFF to ON blocks which results in Unambiguous results . And retention cells are used for the storage purpose of the previous values which is required for further computation. So for retention Strategies Registers are used for storage, Isolation cells might me AND, OR gates or latch. And these cells are inserted based on the Requirement of the design specifications.

The design is implemented using UPF is shown in fig (6)

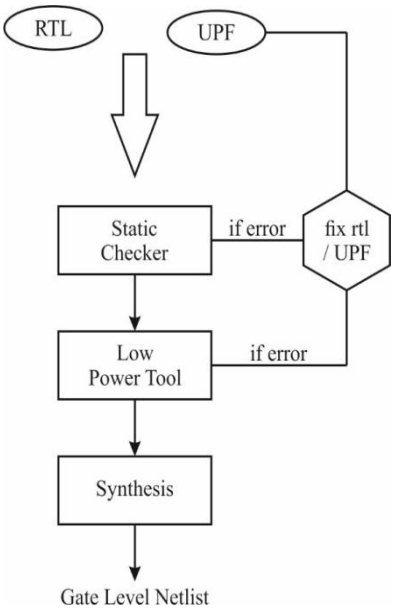


Fig. 6 Power Format Design Implementation Flow Chart

Fig. 6 shows how the complete design flow is carried out. From RTL level to synthesis and the results are compared with CCLA and SCBCLA with and without UPF.

7 Results and Inference

ASIC Implementation of Semi-custom design of different designs of CCLA and SBCLA along with the usage of UPF is implemented and the corresponding readings i.e. area and Power estimate are noted and are as follows:

Table 1. Average area and Power calculations for CCLA

Design	**Area (μm^2)**	**Switching Power (µw)**	**Switching Power With UPF (µw)**
Hybrid CCLA_1	349.6702	5.7741	5.3318
Hybrid CCLA_2	347.61	5.6145	5.3690
Hybrid CCLA_3	349.93	5.7168	5.2985
Hybrid CCLA_4	352.12	5.745	5.322

Table 2. Power and area calculations for SCBCLA

Design	**Area (μm^2)**	**Switching Power (µw)**	**Switching Power With UPF (µw)**
Hybrid SCBCLA_1	349.6702	5.7741	5.3318
Hybrid SCBCLA_2	347.61	5.6145	5.3690
Hybrid SCBCLA_3	349.93	5.7168	5.2985
Hybrid SCBCLA_4	352.12	5.745	5.322

Above Table 1 and Table 2 contains the tabulated results of the Area, power calculations of CCLA and SCBCLA with and without UPF. Here we can evaluate the performance in terms of power and area. Table -2 shows there is reduction of power and area and is better observed in fig -7.

1. Area of the design is decreased in SCBCLA compared to CCLA architecture
2. When power is compared when compared to switching power for normal design to design with UPF almost in this pivoted chart with SCBCLA there is around 14 to 18 % decrease in switching power which results in better power optimization.

3. Fig-7 shows the Pivotal chart where it represents the power comparison of the design without UPF and with UPF and hence we can summarize that UPF provide reusability of Code in order to obtain better performance of the modern complex digital designs.

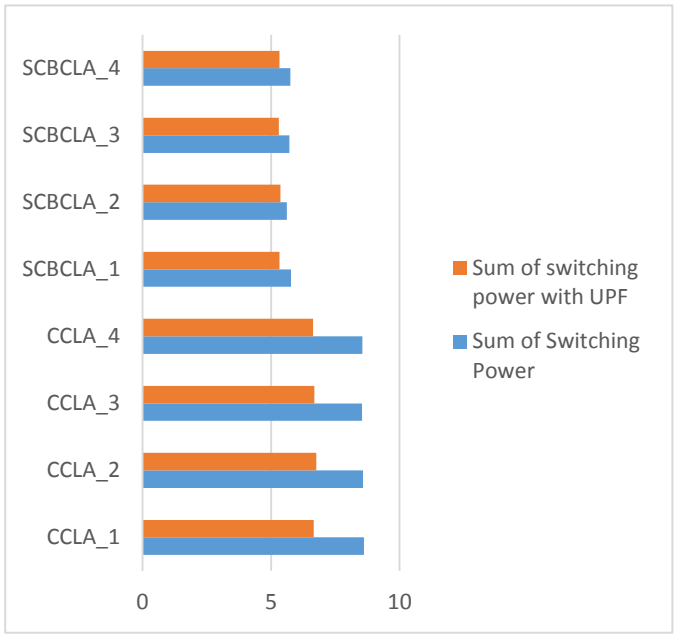


Fig-7 pivotal chart

8 Conclusion

The objective of the proposed work is to build an efficient low power, area VLSI architectures utilizing the efficient power management technique that depends on the correct power management strategies for efficient power architecture decision-making. An efficient design methodology is introduced by the power format at the circuit level by adding and verifying the power intent and managing the design to provide its figure of merit into the design architecture. Using these techniques we can step forward to design or manufacture efficient power management systems even with structural dependency architectures.

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