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Fault Analysis of HVDC Converter Based on Alternate Arm Converter Topology

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Abstract

Recent advancement of High Voltage Direct-Current (HVDC) transmission based on alternate arm converter (AAC) draws the attention of researchers due to their unique structure. It is a hybrid converter as the characteristics of this converter varies among the modular multilevel converter (MMC), due to the existence of H-bridge cells, and the two-level converter, in the sort of director switches in every arm of the converter. AAC presents the improved fault tolerant characteristics compare to traditional voltage source converter (VSC). It has gained much popularity in HVDC transmission because of its robustness against fault, ability of generating superior ac voltage compares to the dc terminal voltage. At this point energy balance between the ac and dc terminal is equal. Therefore, the significant contribution of this paper is to analyze the performance of AAC model under normal condition and fault condition which proves the robustness of AAC converter against the faulty situation. Both AC and DC faults are considered in this study. Simulation is performed in Matlab/ Simulink environment.

Keywords: Alternate arm converter, Energy Balance, H-bridge Cells, High Voltage Direct-Current, High Voltage Direct-Current

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1 Introduction

The demand for electric power is increasing very fast in the world, but the energy is often harvested far away from the consumption in order to use energy sources with less environmental impact. This has encouraged the development of power system solutions for large bulk power transmission. High Voltage Direct Current (HVDC) is a technology used for transmission of large amount of electric power, depends the on line commutated converters, but the development of power semiconductors has enabled the use of self-commutated converter technology which has encouraged the growth of renewable resources such as offshore wind farms [1].

Since 1990s, a substantial amount of research project has been investigated to improve the performance of converters that will create them further power efficient compare to the existing first generation VSC. Detailed literature of the improvement of AAC converter has been given in [2-4]. Modular Multilevel Converter (MMC) has been investigated for power system with STATCOM application at the end of 20th century and for HVDC network in 2003 [5] and developed more in [6], brought the new topology of VSC. Being a novel system of VSC converter, MMC uses the stack of alike sub-modules (SM) rather than the switching series of the orthodox two or three level VSC. 1st MMC-HVDC research project, named as "Trans Bay Cable Project" proposed in USA, has successfully started their commercial commission in high voltage system. Existing MMC converter requires enough sub-modules to be able to produce entire dc voltage. However, due to the large structure and more semiconductor devices, power loss also more in those converters [7]. AAC converter has modular structure with good voltage control mechanism, acceptable THD with low switching frequency and reduced losses. It has also the ability of DC-fault Blocking and thus improve the performance of the converter [8]. Moreover, Alternate Arm Converter (AAC) can operate under faulted AC-grid conditions [9-11]. Because of the significant advantages of AAC, the main focus of this research is to develop a model to investigate the performance of AAC under normal and faulty conditions. It has been proved that, AAC can perform well against the faulty situation and thus proved its importance to apply in HVDC applications.

Rest of the paper is organized as follows. Section 2 and 3 describes the details of AAC topology. Section 4 illustrates the case study with simulation result of AC and DC faults. Finally, the paper is ended with conclusion in section 5.

2 Description of Proposed Topology

An Alternate Arm Converter (AAC) is proposed in [3], which is actually one type of a modular multilevel VSC. This converter is a hybrid topology that integrate the characteristics of both 2-level and multi- level converter. Figure 1 illustrates the proposed AAC where each phase-leg of the AAC consists of a positive (upper) and negative (lower) arm. Both arm of the converter includes a mass of H-bridge cells, a director switch and a little arm inductor. The director switch is formed from a series connected IGBTs. The key role of the director switch is to select the arm which can conduct the AC current. As H-bridge cells have been used in this converter, voltage developed by the stack of cells can be either optimistic or unenthusiastic, thus if required, the converter can shove its AC voltage higher than the DC terminal voltage. Peak voltage that each stack of cells of the converter has to yield equals the half of the DC bus voltage. The full bridge and half bridge cells are depicted in Figure 2. So, the objective of the proposed AAC is to decrease the number of cells, IGBT and hence the losses of the converter. AC-side of the AAC is connected with the wye-delta transformer and is set to minimize the DC circulating current.Therefore, the converter needs to operate so that the total amount of energy converted from the AC side equals the total amount of energy delivering to the DC side. To obtain this goal, the converter needs to be operated to maintain the zero net energy swap for the stacks over each half sequence.Energy exchange between the AC and DC side depends on the difference between the quantity of energy released from the AC side and entered to the DC-side.

$$E_{ac} = \int_{0}^{T/2} V_{ac}(t).I_{ac}(t).dt \quad (1)$$

$$E_{dc} = \int_{0}^{T/2} V_{dc}/2.I_{ac}(t).dt \quad (2)$$

Now, by equating the total amount of both energies absorbed and energy release, an ideal operating point can be identified. It is mentionable here that, the magnitude of peak AC voltage is superior than half the DC bus voltage. It directs the converter to use the cells in the opposite direction.

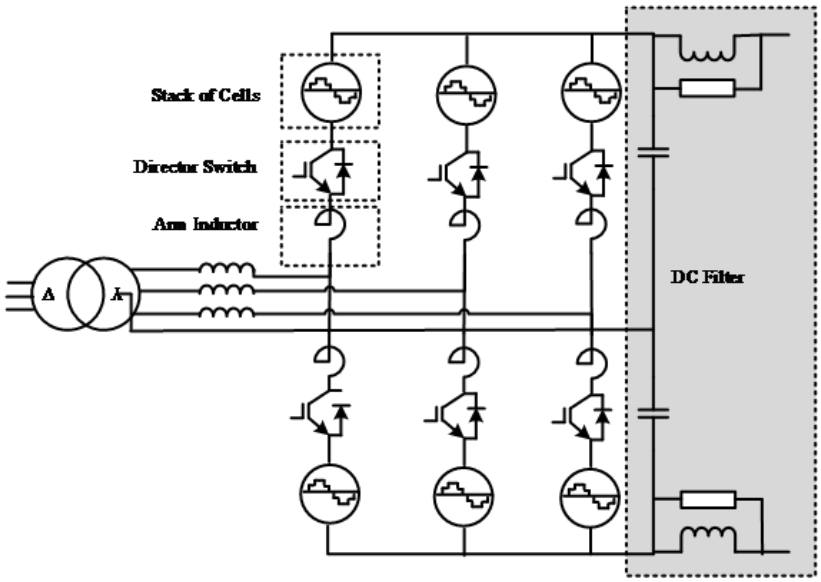

Figure 1 Diagram for Alternate Arm Converter [3].

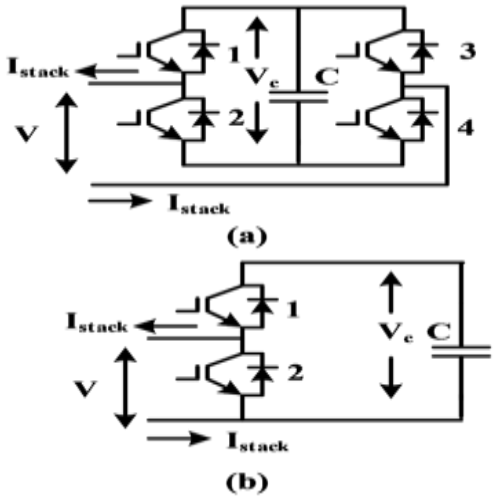

Figure 2 (a) Full-bridge and **(b)** half-bridge cell configuration

3 DC Fault Ride Through and STATCOM Operation

When a significant DC voltage depression occurs or a complete short circuit takes place, then it is required for the converter to continue its operation. It can be observed if STATCOM provides voltage support to the AC system keeping the AC/DC power transmission mechanism disabled. The choice of operation of director switch can be depicted as

shown in Figure 3. In AAC, during the DC side fault the operation may be of several types: one arm conducts per half cycle likewise the typical operation (A), one arm functions uninterruptedly (B) or two arms work together (C), and potentially improve the reactive power capability.

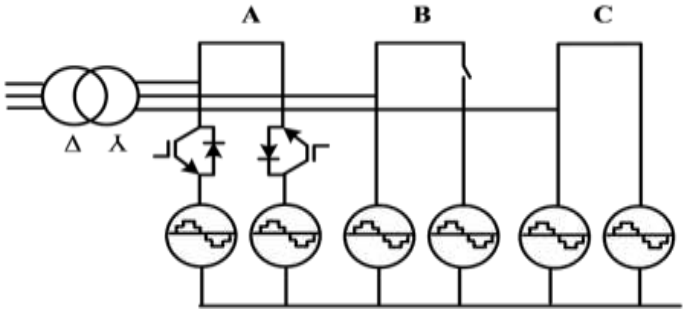

Figure 3 Modes A, B and C of the AAC during DC-side fault

4 Simulation Results

4.1 Case Setup

Two separated electrical networks are planned to be connected with an HVDC-link between them in order to increase the flexibility and enable the trading with electricity. The model used in this study is depicted in Figure 4. At the prospective location of the interconnection, the two grids are separated by a 300 km wide ocean bay. In order to settle the procedure of this AAC, a Simulink representation has been developed in MATLAB Simulink environment. The key parameters of the developed model are summarized in Table 1.

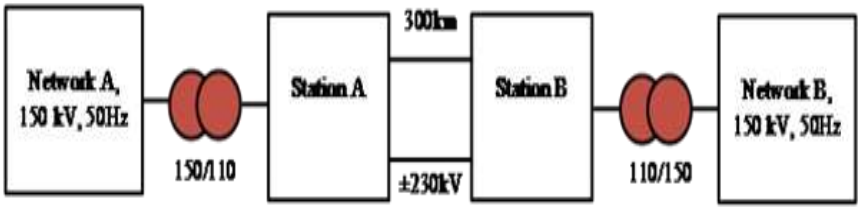

Figure 4 HVDC System based on AAC Converter

4.2 Performance under Normal Condition

The HVDC AAC model simulation under normal condition is performed initially to compare with the result when it operates under faulty condition. Simulation results under normal condition are depicted in Figure 5.

Table 1 Selected variable parameters and levels

No	Corresponding values of system components	
	Characteristics	values
1	Active and Reactive Power	5 MW and 20 MVAR
2	Dc Bus Voltage	230 kV
3	Grid side AC voltage	110 kV
4	Converter side AC voltage	150 kV
5	Arm Inductance, Cell Capacitor	0.5 mH, 4 mF
6	Inductor, Capacitor	6 mH, 1.68 mF
7	DC Filter Resistor	2.66 Ω
8	Stacks, Direct Switches	6 cells, 6 IGBT's

From the simulation we observed following points:

i.The converter output shows that, the dc voltage and the current are stable.

Within the same time period, the inverter side AC voltage and the inverter current also stable as there is no fault. Although there is some initial fluctuation, no significant deviation of voltage and current have been observed.

ii.From the FFT analysis of inverter current it shows that, the current is high quality with low THD (3.51%).

iii.The initial fluctuation of the DC grid voltage, dc current and inverter current

have been restored and stabilized in the original value within a short period

of about 0.2s while charging the capacitors.

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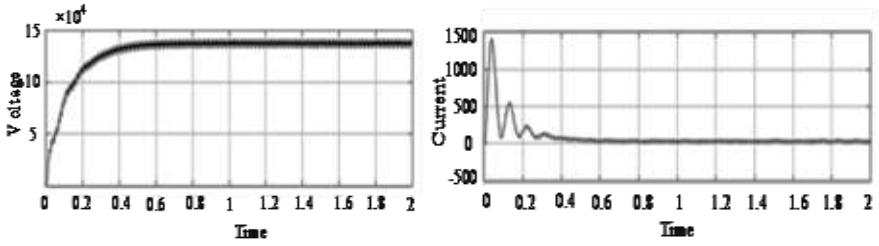

(a) (b)

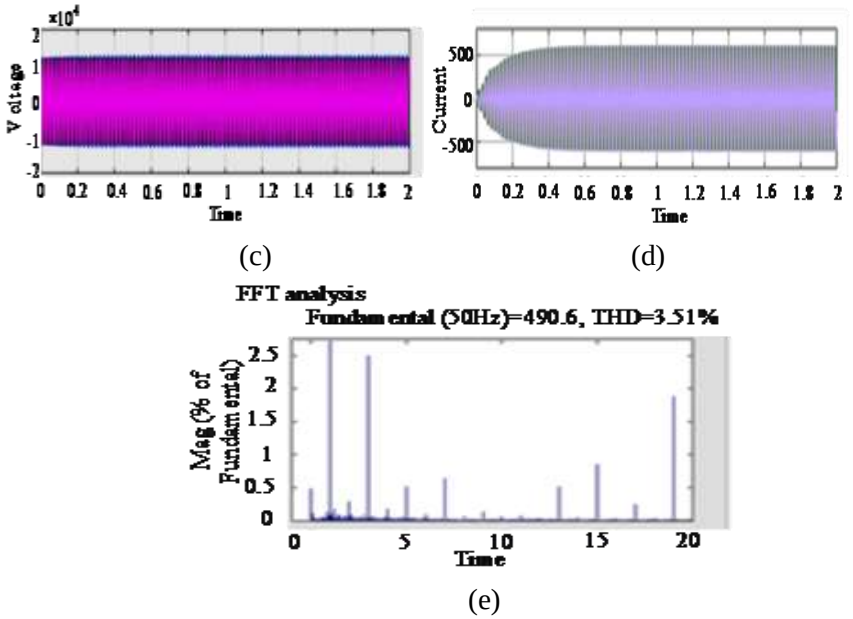

Figure 5 AAC Simulation Under Normal Condition. **(a)** DC Grid Voltage **(b)** DC Current **(c)** Inverter side ac Voltage **(d)** Inverter side AC current **(e)** FFT analysis of inverter side current.

4.3 Performance under DC Fault

To observe the ability of dc fault blocking capability a DC pole to ground fault is applied between 0.6s to 0.9s. The simulation results under this condition are plotted in Figure 6.

From the simulation following points have been observed:

i. When DC voltage collapse to zero a current spike formed to discharge the DC bus capacitor. During the fault time within 0.6 to 0.9s, the dc voltage deviated, and the dc current also shows some fluctuation till the fault clears. The dc voltage and current also returned to their original position after the fault time.

ii. During the fault time, DC filter behaves like RLC circuit with pre-charged Capacitor & inductor.

iii. However, during dc voltage collapse, active power transfer is set to zero. Hence, AAC inject reactive power to support the AC grid acting as STATCOM. Therefore, the inverter voltage has no change, although there is some fluctuation in the inverter side ac current. As the fault has been cleared at 0.9s, the inverter current also restored by this time.

iv. When DC fault is cleared, AAC has resumed its normal operation instantly. Overall, during the fault time, the dc voltage and current have some distortion, however, the inverter voltage shows constant voltage.

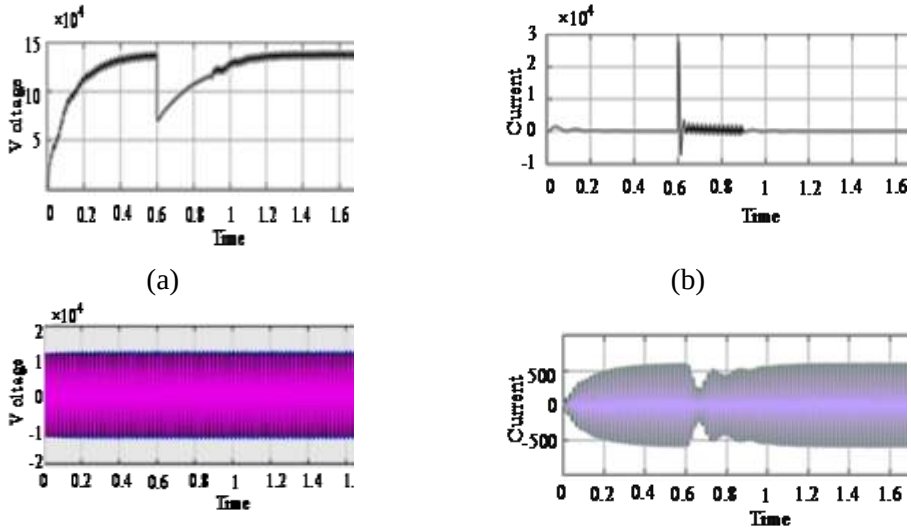

Figure 6 5 MW AAC simulation Under DC Fault between 0.6s to 0.9s. **(a)** DC Grid Voltage **(b)** DC Current **(c)** Inverter Side AC Voltage **(d)** Inverter Side AC Current.

Ref [2] analysed the dc fault blocking capability with 9 stack cells and 9 IGBT's. Obtained results showed that the voltage was fluctuated from the rated 10kV and the inverter side current also shows ripple. In this research, a new topology is proposed with 6 IGBT's and 6 cells which shows stable output voltage of 20kV and quick recover capability of inverter side current after 0.9s. During normal operation of the proposed topology, the dc voltage had no fluctuation and the dc current also stable. However, during the fault conditions, when the fault occurs, the dc voltage drops suddenly and again it reaches its original position after the fault clearance. The dc current shows sudden increase in this time, though it regains its original position swiftly.

4.4 Performance under AC Fault

To observe AAC under ac fault condition a three phase to ground fault is applied between 0.6s to 0.9s. Obtained results under AC faults are shown in Figure 7.From the simulation we observed following points:

i. AAC performs well during symmetrical three phase fault as the voltage and current output of inverter restored swiftly after the fault is cleared. In this case, the dc voltage and the current show the similar performance likewise under normal condition. Hence, no change in the output waveform as the fault is in AC side.

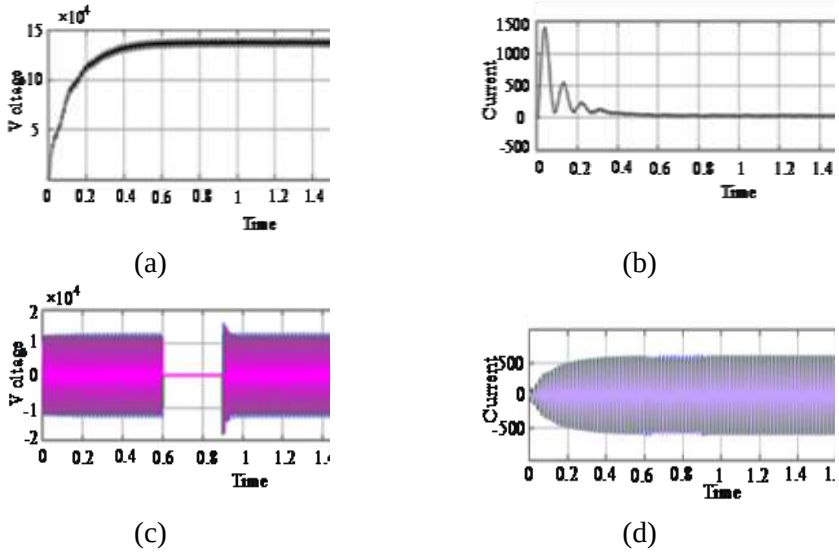

Figure 7 5 MW AAC simulation Under Three phase AC Ground Fault Between 0.6s to 0.9s. **(a)** DC Grid Voltage **(b)** DC Current **(c)** Inverter Side AC Voltage **(d)** Inverter Side AC Current.

ii. The AC voltage has turned to zero within the fault time 0.6 to 0.9s. Again, it has been restored after this period. The inverter current also shows slight deviation during this time. However, it has also returned to the desired value after the fault is cleared. Overall, the robustness of the proposed topology is proved during the faulty conditions of the converter.

The analysis proved that; the ac fault has no influence on the DC side like we have observed under the dc fault conditions. Hence, the dc voltage and current shows similar response as it showed on normal operation. However, the inverter side AC voltage has been reduced to zero volts when the fault occurs and again it has reached at 20kV after the fault clearance at 0.9s. It means, the dc faults and ac faults have the effect on dc and ac side, respectively, keeping the other side unaffected, which proves the robustness of the proposed converter.

5 Conclusion

In this research performance of AAC has been observed to prove its application in HVDC transmission line. For this purpose, the converter performance has been evaluated under faulty conditions. Both DC and AC

faults have been observed in this study. Obtained results reveal that, the converter performs satisfactorily under faulty situations. Therefore, the significant contribution of this research is to prove the robustness of AAC converter against the faulty conditions. Director switch of the AAC converter reduces the number of sub-modules, therefore, the total number of diodes reduced compare to existing MMC converter. Subsequently, the total loss also reduced. The future scope of this research is the application of AAC for the large scale power system in domestic and industrial applications.

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