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Improving the System Thermal Reliability Using Thermal-Gradient-Based Placed Heaters

[1]Sherif Hany, [2]Shohdy Abdel Kader, [3]Hany Fekri Ragai, [4]Emad Hegazi

[1,2,3,4]Electronics & communications department, Faculty of Engineering, Ain Shams University, Cairo, Egypt.
E-mail:12777@eng.asu.edu.eg,shohdya@gmail.com, hani_ragaai@eng.asu.edu.eg,emad.hegazi@eng.asu.edu.eg

Abstract

Design reliability requirements are growing rapidly to cope with design complexity and process challenges. Common design specifications are qualified against process corners, known as PVT (process, voltage, and temperature), are getting more complex. Bias, bandgap, circuit is one of the critical building blocks which compensates for both supply fluctuations and temperature variations. In these bias circuits, the incorporated temperature compensation techniques are usually based on first or second order approximations which reduce the temperature validity range. Beyond this validity range, the biasing reference voltage gets dominated by nonlinearities and becomes temperature dependent. The impact of these nonlinearities is amplified by the effect of thermal gradient across the chip which causes both soft and hard silicon failures. This work proposes an on-chip temperature sensing and holding mechanism that extends the bias temperature compensation validity range by keeping the chip in thermal equilibrium and avoiding thermal gradient and skewness. This work leverages a geometrical-based thermal symmetry and gradient verification approach that allows even placement and distribution of thermal heaters in low voltage (LV) areas to compensate for hot regions across the chip. The flow has been implemented on a voltage regulator test chip and demonstrated reliability improvements.

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1 Introduction

Modern IoT and automotive applications involve complex design and process requirements. The design complexity arises from the presence of multi-power domains, high current densities and other reliability specifications related to the SoC ability to absorb supply fluctuations and temperature variations. This causes thermal failures which became more significant in new high density chips due to the diminishing role of cooling mechanisms. The process complexity emerges from new manufacturing steps such as multi-patterning techniques that are required to enhance minimum features printability. These new manufacturing techniques do not only impose advanced electrical and thermal matching requirements but also increase the number of required masks as well as the count and permutations of device corners. These PVT (process, voltage, and temperature) corners describe all device variabilities in terms of dimensions, operating conditions, supply fluctuation and temperature variation.

Different techniques are used to reduce the impact of PVT corners. Process corners (P) are commonly solved by layout design techniques such as common centroid and device shielding. On the other hand, supply fluctuations (V) and the temperature variations (T) compensation require a dedicated circuit called bias circuit –also known as bias cell or bang gap circuits.

Bias circuits regulate supply fluctuations (V) by incorporating self-biasing techniques in addition to leveraging operational amplifiers gain-bandwidth specification. The quality of supply fluctuations rejection is measured by power supply rejection ratio (PSRR). However, temperature compensation techniques are not as simple since their implementation involve approximations which limits the region of validity. The bias circuit generates a temperature-independent voltage by adding a PTAT and CTAT (proportional/complementary-to-absolute-temperature) currents which have positive and negative temperature coefficient respectively. Figure 1 shows PTAT and CTAT currents compensating each other over a narrow validity range. Outside this validity range, the nonlinearities dominate thermal behavior and the reference voltage becomes temperature dependent [1].

The significance of these nonlinearities is very pronounced in applications that has high contrast in thermal regions such as high power/voltage (HV) applications where HV regions tend to get hotter faster than their low voltage (LV) counterparts. Similarly, for high speed/frequency analog mixed signal (AMS) designs where the digital portion is bulky and consumes relatively high dynamic power compared to the analog counterpart. In these applications the impact of the narrow temperature compensation validity range is significant due to temperature skewness and large thermal gradient [2, 3]. This forces the chip to take finite time to reach equilibrium as shown

in figure 1. This skewness has recently been manifested, based-on silicon measurements, in the form of soft and hard failures. Soft failures occur when the temperature dependencies push devices out of temperature lock–in range increasing the bias cell settling time. When the shift from designed operating temperature is large, the bias cell fails to lock and settle causing hard failures.

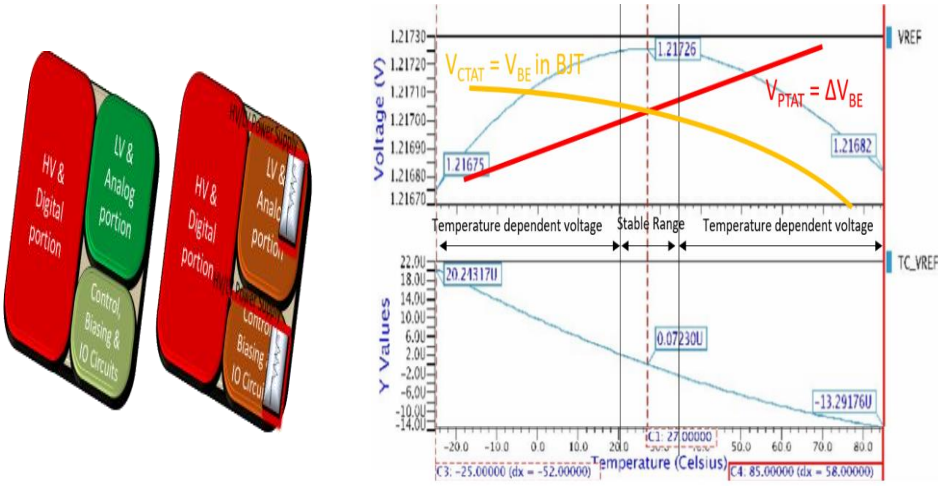

Figure 1 Tradition Full Chip Heat Map with No Heaters Showing Thermal skewness/gradient (left) and chip in equilibrium either after settling or incorporating heaters aiming for faster settling time and wider temperature compensation and stability range (right). Note: the color code used shows dark red as hot region and green as cold one.

Traditional thermal gradient fixing techniques tend to increase spacing between HV devices allowing air flow, implement cooling mechanism and other approaches that reduces the thermal hotspots and gradients. However, the efficiency of such thermal relief techniques are diminishing in new designs due to high device density and large metal stacks. Also, the presence of multi-power domains in addition to smaller feature/devices dimensions increase the current densities causing more heat dissipation and larger thermal gradients. This work proposes an on-chip temperature sensing and feedback mechanism that keeps the across chip temperature in equilibrium and ensures valid bias circuit operating conditions using a voltage controlled thermal resistors/heaters. The concept and specifications of the heater is covered in section 2. Sections 3 and 4 demonstrate the design and verification methodologies respectively to drive the thermal gradient and ensure even heaters distribution. Section 4 also covers the traditional approaches used to fixing and validating thermal gradients. Finally, section 5 covers the results while Section 6 summarizes and concludes the work.

2 Methodology Overview

The proposed methodology shown in figure 2 incorporates an on-chip temperature sensing that drives voltage-controlled resistors called “Heaters”. These resistors heat up the LV cold areas and allow the chip to reach thermal equilibrium faster whenever the chip restarts due to cycle slipping, power surge or any event that causes thermal gradient. Once the equilibrium is achieved, the heaters are powered down to minimize the leakage.

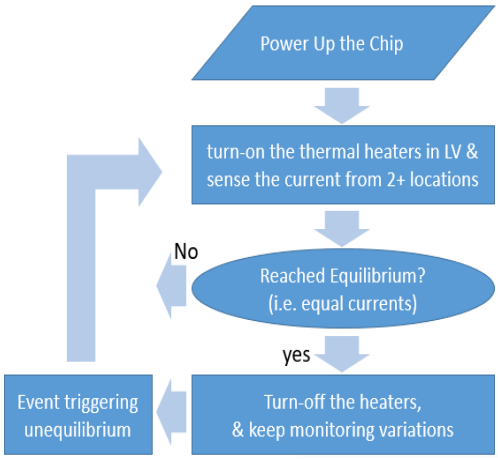

Figure 2 Methodology of Operating Thermal

The heaters are voltage controlled resistors that dissipate current and convert it to heat energy to heat up the targeted part of the chip. Due to the novelty of this approach, this section covers different aspects of designing the heaters as follows:

1. Heater electrical specification: the heaters power consumption should be significantly small. These heaters are expected to be turned on by a small current for short period of time to deliver the required heat till equilibrium. Also it should minimize the leakage current when powered off. The amount of heat generated and dissipated by these heaters is dictated not only by current dissipated in resistance but also by the resistivity ($W/^{o}K$) for the material which required testing several resistor types; Nwell, Polysilicon, and metal resistors.
2. Heater physical placement specification: this considers the heater proximity to a power supply and sensitive circuit. Having HV supply routed through LV domain might cause reliability complications that need extended HV spacing especially for voltage-dependent DRC [4]. Another reliability consideration is related to the fact that the heaters should be placed away from critical blocks that might be impacted by extra heat and can degrade over time.

3. Heater placement and thermal distribution: this is related to the precise relative locations of the heaters with respect to the original heat sources. The heaters placement should ensure even thermal distribution as well as achieving equilibrium fast [3]. Although the initial impression is that this will increase the overall chip temperature and power dissipation, the flow just turns on the heaters for a short period of time consuming minimum power and switches them off once the equilibrium is achieved without impacting the overall temperature.

3 Implementation

The system implementation is part of a 0.18um testchip where the bias cell is powered by 1.8v supply, produces biasing currents of 50 µA - 200 µA for multiple blocks. The V_{ref} PSRR is -31db, the setting time is 1.9502 µseconds and the total power consumption (with heaters OFF) of 1.52 mWatt. The heaters and their associated circuit adds 0.18mW which is about 22% power consumption increase for the bias cell.

An on-chip sensing system with a thermal feedback loop is shown in figure 3 where the heat is sensed by the temperature sensor in LV region and triggers the logic which in turn adjusts the voltage-controlled heater. The system components are as follows:

1. Temperature sensors: This circuit is a variant of the bandgap circuit known as Brokaw circuit [4]. The temperature sensing uses the PTAT current as an indication of temperature change. This then drives an on-chip analysis and tuning functions. Figure 4 (left) shows a conceptual schematic of PTC generation circuit used for temperature sensing. An Operational trans-conductance amplifier (OTA), shown in figure 4 (middle), uses miller compensation technique demonstrating a phase margin of 68o and high gain margin 78db to allow for both loop stability as well as power supply rejection ratio (PSRR) which shows the ability of the bias circuit to absorb supply fluctuations.

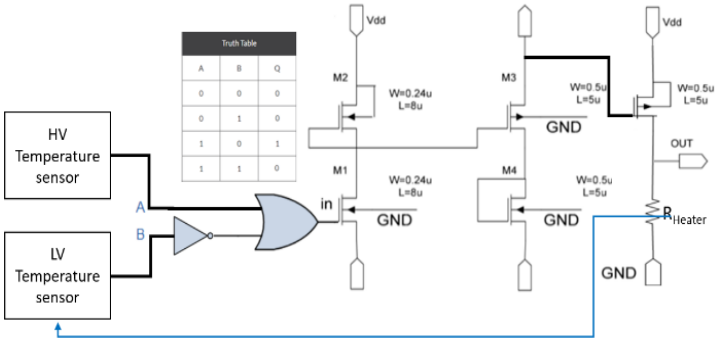

Figure 3 Complete System with Main Heater & Thermal Feedback Loop

2. Control logic: A simple Boolean circuit is implemented with voltage restorers to provide binary control to the heater circuit. Recent on-chip thermal/power sensing techniques as in [5] use advanced controlling mechanisms that involves machine learning.
3. Voltage controlled heater (figure 3): the heater circuit behavior is similar in concept to the traditional start-up circuit. Figure 4 (right) shows a typical circuit:

- Originally the start-up circuit is used to activate the circuit and move it away from a passive stable state where zero currents (degenerate bias point) exist and excites an intermediate node for a very short period of time to move to the actual operating condition. The same concept is used to control the heater where presence of DC path between VDD and GND supplies a small current initially -or when control logic output is zero- then it shuts down to allow for normal operation of the rest of the chip which happens during equilibrium.
- Both the start-up current and voltage-controlled heater power consumption should be minimal during OFF mode to avoid leakage while they should dissipate enough heat when turned ON to reach equilibrium faster.

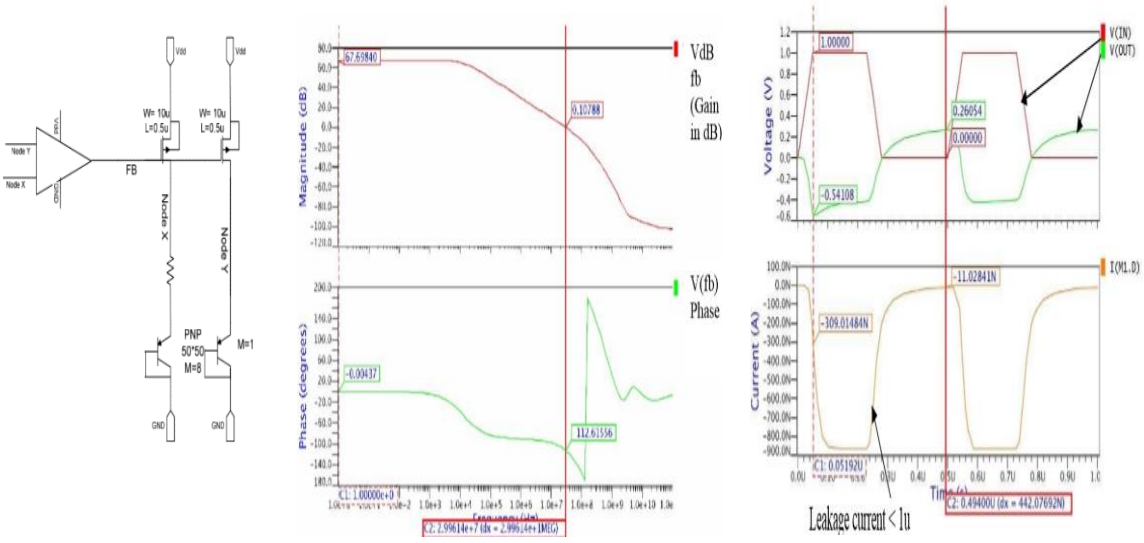

Figure 4 (left) Heater Current consumption for ON/OFF modes. (Middle) PTC Circuit Temperature Sensor & (right) OTA Response

4 Proposed Verification Methodology vs Traditional Approaches

The heaters are placed in locations that do not only address thermal gradient issues but also considers heat source distribution. The traditional approaches for verifying the thermal gradient and heat distribution involve either thermal/electro-thermal simulations or thermal-aware placement tools. Both of these approaches are not present in traditional design flows. The former is known as "Relaxation" and it requires modeling the temperature skewness and its impact on operating condition before alternating between thermal and electrical simulator till convergence. The latter approach is a thermal-aware layout placement approach [2, 6] where the heat source placements accommodate thermally-induced mismatches and iteratively optimize the thermal profile. This approach is usually tied to specific design environment/tool in addition to the long runtime, medium capacity and generally lack of standardized flow.

In this work, a thermal placement verification flow [7] is implemented to analyze thermal placements from geometrical perspective with no need for complex simulations. The verification flow identifies HV active devices and the voltage controlled heaters as the main source of heat. Then the device seed layers get annotated by current or power consumption based on a DCOP (operating point) analysis. Equivalent device seeds are clustered together based on their proximity, hierarchical interaction, connectivity, and other electrical parameters. Isothermal kernels surrounding the heat sources are superimposed to derive the thermal profile. The flow analyzes the thermal gradient to allow back-end designers to interactively adjust the heaters placement aiming for even thermal distribution as shown in figure 5.

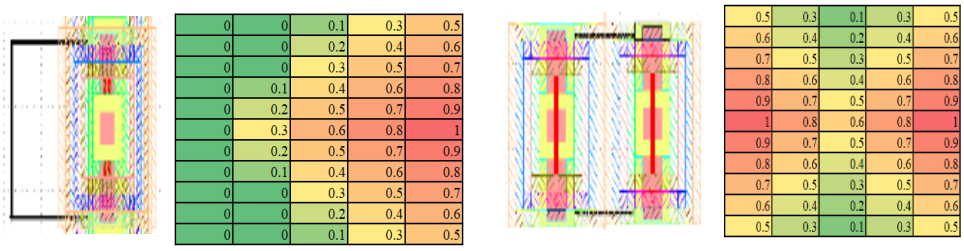

Figure 5 Heat Map Showing Heat Source Distribution and Thermal Gradient Violations (Left) and (Right) After Smoothing.

5 Results

A real medium size design 0.5mmx0.3mm is used as the testing vehicle. There are 803 heat sources, namely, devices that consume high current. Figure 6 shows the chip thermal profile highlighting thermal hotspots and thermal gradient issues related to LV and neutral zones on the chip. The

hotspot analysis, thermal symmetry analysis and the thermal gradient checking is based on the technique in [7].

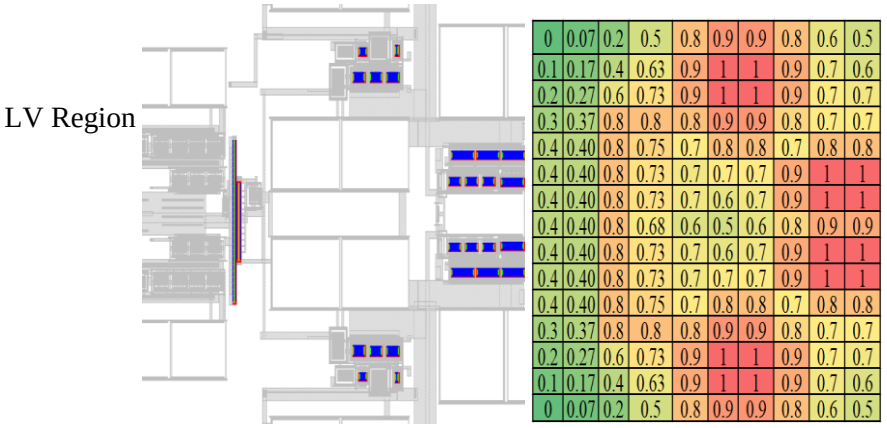

Figure 6 Full Chip Thermal Profile Showing LV Area on the Left that is Causing Thermal Gradient Issue.

The implemented flow provides actionable feedback to the designer to fix thermal gradient issues by adding thermal resistors as shows in figure 7. The thermal heaters are sized to dissipate the same amount of current as their HV counter parts and evenly placed to solve the thermal gradient issues. It is worth noting that figure 7 is the normal operating mode of the chip after equilibrium. In other words, the implemented heaters allow reaching equilibrium faster without increasing the overall chip temperature.

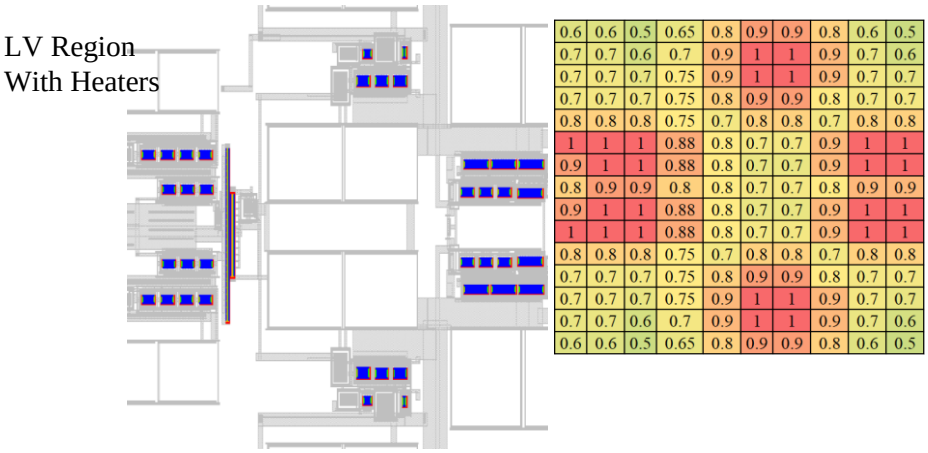

Figure 7 Full Chip Thermal Profile after Fixing Thermal Symmetry and Gradient Issues by Adding Heaters in LV Region

6 Conclusion

This work enhances the system robustness and reliability by improving the biasing circuit responsible for providing temperature-independent reference voltages. The proposed flow allows for faster thermal equilibrium avoiding thermal gradient issues which causes skewness and has recently been proven as a new failure mechanism. An on-chip sensing and correction technique is presented covering the voltage-controlled heater circuit specification, implementation, initial results, and explanation for the incorporated approximations and heuristics.

This work also presents an enhanced thermal validation utility that performs thermal-like analysis. This geometrical-based analysis provides a rough heat map showing thermal hotspots as well as thermal gradient violations. The flow provides an actionable feedback that allows interactive verification of these violations and ensures even heaters distribution very early during the floor planning stage.

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Biography

Sherif Hany Mousa received both his B.Sc. and M.Sc. degrees in electrical and communication engineering from Faculty of Engineering Ain-shams University in Egypt in 2007 and 2013 respectively. Currently, he is perusing his PhD in the same university in the field of structural techniques for analog design for testability and circuit analysis. From 2007, he worked as QA/R&D engineer as part of Chameleon ART tool at Mentor, A Siemens Business, then assumed a role of IC design consultant and physical verification ruled deck writer till 2010. Since then, He has been part of Mentor Calibre product team as principal technologist for physical, circuit and reliability verification. He has several publications and patents in the field of analog layout porting, DFM, hotspots detection and analysis using Calibre DRC, Calibre PERC and Calibre pattern matching.

Shohdy Abdel Kader, Electronics & communications department, Faculty of Engineering, Ain Shams University, Cairo, Egypt.

Hany Fekri Ragai, Electronics & communications department, Faculty of Engineering, Ain Shams University, Cairo, Egypt.

Emad Hegazi, Electronics & communications department, Faculty of Engineering, Ain Shams University, Cairo, Egypt.